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10/602,020	06/24/2003	Frederic Reblewski	003921.00135	7641

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EXAMINER	
SAXENA, AKASH	

ART UNIT	PAPER NUMBER
2128	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/602,020	REBLEWSKI ET AL.	
	Examiner	Art Unit	
	Akash Saxena	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/24/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-31 have been presented for examination based on the application filed on 24th June 2003.

Information Disclosure Statement

3. The information disclosure statement (IDS) submitted on 24th February 2005. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the examiner is considering the information disclosure statement.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding Claim 1

Claim 1 discloses a method for compacting state data whereas there are no steps are recited in the claim that perform data compaction, hence the claimed steps do not meet the goal recited in the preamble. Even if it is assumed that the step of sorting is doing the compaction, still there are no limitations provided to clarify how such a sort is achieving the compaction of state data.

Further, the step of storing the first sample data and the step of determining the residual space do not correlate. It is not clear if the sorted data is stored in the first buffer, which is determined to be empty. Further, if the first buffer does not have residual space, no indication is provided where the data is stored.

Above deficiencies make the claim vague and indefinite.

Claims 2-19 are rejected based their dependence on claim 1.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 1-17, 19-26 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Application No. 09/920930 by Kurooka et al (Kurooka hereafter), in view of U.S. Patent No. 6,816,989 issued to Timothe Litt (Litt hereafter).

Regarding Claim 1

Kurooka teaches compacting state data of an emulation system (Kurooka: [0006][0028]), by receiving a first sample of state data (Kurooka: [0023][0024], Fig.1), sorting the first sample as compressing the data (Kurooka: [0006][0028][0039]), storing the sorted first sample (Kurooka: Fig.1, trace buffer A & B [0026]).

Kurooka does not teach explicitly determining if residual storage space in a first buffer exists.

Litt teaches determining if residual storage space in a first buffer exists as smart buffers, which are aware of the buffer state (full or available) of each location in the smart buffer (Litt: Col.10 Lines 12-46). Litt also teaches receiving a first sample of state data (Litt: Col.8 Lines 33-48), sorting the first sample (Litt: Col.7 Lines 20-67), and storing the sorted first sample in the smart buffer (Litt: Fig.2). Although not claimed as the method step the preamble states compression of the trace data. Litt does not teach compression in the manner taught by Kurooka.

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Litt to Kurooka. The motivation to combine would have been that Litt and Kurooka are analogous art both concerned with trace data capture coming in at higher rate than it can be shipped out to external trace storage (Litt: Col.2 Lines 52-65; Kurooka: [0009]). Kurooka solves

the problem by handling various data sizes by compressing the data (Kurooka: [0006][0028][0039]) and Litt by prioritizing the data and dropping the less relevant data packets (Litt: Abstract).

Regarding Claim 2

Litt teaches the step of determining whether the first buffer is full and storing the sorted first sample in the first buffer (Litt: Col.10 Lines 17-46).

Regarding Claim 3 & 4

Kurooka teaches portioning the sorted first sample into two portions and storing a portion in the first buffer and storing the remaining portion in the second buffer (Kurooka: Fig.5 - Splitting and interleaving the Input data between the trace buffer memories A, B and C). Another embodiment teaches filling in the trace buffer memory A first without interleaving with other memories (Kurooka: Fig.6-7).

Regarding Claim 5

Litt teaches filling up the smart buffer and compaction of the data (Litt: Col.10 Lines 47-60).

Regarding Claim 6

Kurooka teaches second buffer assumes the role of the first buffer and the first buffer assumes the role of the second buffer as alternating the trace buffer memories A and B while storing the data and then empting them (Kurooka: [0042]-[0045])

Regarding Claim 7

Kurooka teaches draining the first buffer into an output storage device as draining the data to the debugger (Kurooka: [0045] Fig 3-4).

Regarding Claim 8

The limitations presented are repetition of the steps performed above in claim 1. They are rejected for the same reasons as claim 1.

Regarding Claim 9

Kurooka teaches portioning the sorted first sample into two portions and storing a portion in the first buffer and storing the remaining portion in the second buffer (Kurooka: Fig.5 - Splitting and interleaving the Input data between the trace buffer memories A, B and C). Another embodiment teaches filling in the trace buffer memory A first without interleaving with other memories (Kurooka: Fig.6-7).
Litt teaches smart buffers that decide based on the residual space left in the buffer whether to store the data (Litt: Col.10 Lines 47-60).

Regarding Claim 10

Kurooka teaches first sample of state data is received from a reconfigurable emulation resource (Kurooka: [0002], [0006]-[0008], Fig.1).

Regarding Claim 11

Kurooka teaches the step of storing the sorted first sample comprises storing the entire first sample in the current buffer (Kurooka: [0045], Fig.3, also in Fig.1).

Regarding Claim 12

Litt teaches sorting of first sample includes both data of interest and ignored data as trace with higher importance and lower importance (Litt: Col.10 Lines 47-60, Col.9). Level of interest is assigned when the trace sample comes into the input multiplexer that contains the parsing logic and prediction logic (Litt: Fig.2 Col.9 Line 45 – Col.10 Line 12).

Regarding Claim 13 & 14

Litt teaches identifying the data of interest from various trace data information using the multiplexer (Litt: Col.8 Lines 33-48). The steps of identifying the bit position within the he first buffer where residual storage space exists and sorting is obvious by description of the smart buffers and packing compaction performed by them, as provided by Litt (Litt: Col.11 Lines 7-47; Col.10 Lines 12-60).

Regarding Claim 15

Litt does not teach explicitly the scenario using the second buffer when there is no residual space available in the first buffer. However, Kurooka teaches alternating the buffers and the using one buffer first (Kurooka: Fig.3-6). Hence the step of using the second buffer is obvious when the first buffer is full.

Regarding Claim 16

Litt teaches step of storing sample information associates with each sample as importance control bit (Litt: Col.9 Line 45 – Col.10 Line 12).

Regarding Claim 17

Litt teaches storing the importance/control of the sample based on the position/length of the sample header. This counter associated stores the bit position of the ticks (segments of the sample – See Col.6 Lines 49-60) of the sample (Litt: Col.14 Lines 5-23; Col.10 Lines 47-60).

Regarding Claim 19

Claim 19 repeats the limitations of claims 1 & 16, where the subsequent packets are stored in the memory and is rejected for the same reasons as parent claims.

Regarding Claim 20

Litt teaches an apparatus having a first select logic device configured to receive samples of state data, to sort samples of state data, and to select data of interest from each of the samples of state data (Litt: Fig.2, Elements 210 & 215, Col.6 Lines 3-34); first and second buffers coupled to the first select logic device and configured to receive the selected data of interest (Litt: Fig.2 Elements 225a 225b); a second select logic device coupled to the first and second buffers and configured to select the first and second buffers in an alternating manner to drain the selected buffer (Litt: Fig.2 Elements 250); and an output storage device coupled to the second select logic device and configured to receive data drained from the selected buffer (Litt: Fig.1 Element 50).

Regarding Claim 21

Litt teaches first select logic comprises a multiplexer (Litt: Fig.2 Elements 245a & 245b).

Regarding Claim 22

Litt teaches second select logic (as arbitration logic) comprises a multiplexer (Litt: Fig.2 Elements 250; Col.11 Line 56-Col.12 Line 43) where the selection between the buffers to offload the data of interest from them makes the use of multiplexer obvious.

Regarding Claim 23

Kurooka teaches filling the buffers in alternating and serial manner as claimed by the disclosed invention (Kurooka: Fig.4-6, [0043]).

Regarding Claim 24

Litt teaches the first select logic device comprises a data of interest sorter (Litt: Fig.2 Packet Prediction and parsing logic with the Prioritization of packets; Col.10 Lines 47- Col.11 Line 6).

Regarding Claim 25

Claim 25 discloses similar limitations as claim 16 and is rejected for the same reasons as claim 16.

Regarding Claim 26

Claim 26 discloses similar limitations as claim 17 and is rejected for the same reasons as claim 17.

Regarding Claim 28

Litt teaches output storage device is configured to store information associated with each of the samples of state data as header to each sample that contains sample relevant data (Litt: Col.6 Line 61- Col.7 Line 19).

6. **Claims 18, 27, 29 30 and 31 rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Application No. 09/920930 by Kurooka et al (Kurooka hereafter), in view of U.S. Patent No. 6,816,989 issued to Timothe Litt (Litt hereafter), further in view of U.S. Patent No. 6,754,599 issued to Gary L. Swoboda et al (Swoboda hereafter).**

Regarding Claim 18

Teachings of Litt and Kurooka are disclosed in the claim 16 and claim 1 rejection above. Litt and Kurooka teach identification of pins for the input source for the first sample (Litt: Fig.2; Kurooka: Fig.1).

Although not clear from the claim language, Litt and Kurooka do not teach identification of *output* pins associated with first sample as understood from the figure in the specification.

Swoboda teaches pin manager and pin macros for identification of output pins where the trace will be outputted (Swoboda: Fig.3-4).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Swoboda to Litt-Kurooka. The motivation to combine would have been that Swoboda and Litt-Kurooka are analogous arts, all concerned with trace data capture. Further, both Swoboda and Litt-Kurooka output the trace data to a debugger (Litt: Fig.2; Kurooka: Fig.1; Swoboda: Fig.3-4) and pin management is obvious for such data offloading. Swoboda explicitly discloses the pin manager, where the pins for trace & debug can be dynamically allocated reducing the limited pin count pressure in offloading trace information (Swoboda: Col.16 Lines 38-63).

Regarding Claim 27

Claim 27 discloses similar limitations as claim 18 and is rejected for the same reasons as claim 18.

Regarding Claim 29

Litt teaches determining a trace data fill rate of each of a plurality of trace data chains as various trace streams with various rates in the bandwidth manager section (Litt: Col.4 Lines 21-25, 55-65); determining a schedule for associating a plurality of pins with the plurality of trace data chains to transfer data out of the trace data chains based at least upon the determined trace data chain fill rates as decision to offload data by the arbitration manager based on the pressure on the trace buffer once it gets full due to higher fill rate (Litt: Col.12 Lines 8-31). Swoboda above discloses the teachings of pin manager.

Regarding Claim 30

Claim 30 discloses similar limitations as claim 29 and is rejected for the same reasons as claim 29. Bandwidth allotment is determined by the arbitration logic and directions from source clock (Litt: Col.12 Lines 57-Col.13 Line 27). Litt does not explicitly teach the pin schedule selection, which is taught by Swoboda (Swoboda: Col.10 Lines 3-4).

Regarding Claim 31

Claim 31 discloses similar limitations as claim 30 and is rejected for the same reasons as claim 30.

Relevance of References Cited

7. U.S. Patent No. 6732307 by Edwards: Edwards is also a close prior art to the claimed invention, as it discloses various trace interleaving methods (Fig.8), details on trace information stored in packetized manner (Fig.7), continuation of second trace sample from next available bit (Fig.8), similar architecture of filtering the data of interest (ie sorting as claimed) (Fig.2, elements 203, 204, 205, 202 and associated explanation).

Examiner's Remarks

8. Applicant's attention is drawn to fig.4A-B, 5A-B and 6A-B. Claim 13 and dependent claims 13 and dependent claims if claimed independently, to reflect the details involved, may be allowable.

Conclusion

9. All claims are rejected.

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

11. **Examiner's Note:** Examiner has cited particular columns and line numbers in the references applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in their entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

    In the case of amending the claimed invention, Applicant is respectfully requested to indicate the portion(s) of the specification which dictate(s) the structure relied on for proper interpretation and also to verify and ascertain the metes and bounds of the claimed invention.

Communication

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Akash Saxena whose telephone number is (571) 272-8351. The examiner can normally be reached on 8:30 - 5:00 PM M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jean R. Homere can be reached on (571)272-3780. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Thursday, December 29, 2005

Fred Ferris
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